UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

H.A

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,662	12/05/2003	Jiro Matsumoto	F00ED0150-DIV	4972

26071 7590 02/27/2007

JUNICHI MIMURA
OKI AMERICA INC.
1101 14TH STREET, N.W.
SUITE 555
WASHINGTON, DC 20005

EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,662	MATSUMOTO, JIRO	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-33,35-44,46,48,50,52,54,56 and 92-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43 and 44* is/are allowed.

6)☒ Claim(s) *1,2,4-33,35-42,46,48,50,52,54,56 and 92-95* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Rejections and/or objections as previously applied

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 2, 6-28, 32-33, 37-42, and 46, 48, 50, 52, 54, 56, 94, and 95 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyajima (JP 2000-299335).

Regarding claim 1, Miyajima discloses in Figs. 14-17 a sealing apparatus for sealing a semiconductor wafer 90 having semiconductor elements on its surface by resin 50, comprising an upper mold 20; and a lower mold 21 having an first area where the semiconductor wafer is mounted, wherein the lower mold having an uneven surface, which is formed within a second area, which is in the first area, and wherein the uneven surface is not formed in the periphery of the first area, as shown in Figs. 1, 16 and 17.

With respect to claim 2, how the uneven surface is formed has not been given patentability weight since claimed invention is directed to a device.

Regarding claim 6, Miyajima discloses in Fig. 17 that slits 98, 76a, 98a, and 77 form the uneven surface.

Regarding claim 7, Miyajima discloses in Fig. 17 that the slits 76a are formed in parallel to each other.

Regarding claims 8 and 9, Miyajima discloses in Figs. 16 and 17 that in the sealing apparatus the area is a first area 21, the slits are formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

Regarding claim 10, Miyajima discloses that the uneven surface is formed by a single spiral slit 98, as shown in Figs. 16 and 17.

Regarding claim 11, Miyajima discloses in Fig. 17 that the area is a first area the single spiral slit 98 is formed within a second area, which is in the first area, and the single spiral slit 98 is not extended to the periphery of the first area.

Regarding claims 12, and 13, Miyajima discloses in Fig. 14 a sealing apparatus further comprising a shock absorbers 78, which are formed under the lower mold 21, buffering stress from the upper mold 20 when the semiconductor wafer is sandwiched by the upper and lower molds, the shock absorbers being disposed symmetrically against the center of the area.

Regarding claims 14 and 15, Miyajima discloses that the shock absorber 78 is formed by a metallic compression spring.

Regarding claims 16, 17, 20, and 21, Miyajima discloses in Figs. 14 and 1% that the shock absorber 78 is a first shock absorber 78,and further comprising a first block 74 having a first recess, the lower mold 21 being contained in the first recess; a second block 76 having a second recess, the first block 74 being contained in the second recess; and second shock absorbers, as shown in Fig. 19, which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

Regarding claims 18, 19, 22, and 23, Miyajima discloses that the second shock absorbers are formed by a metallic compression spring as shown in Fig. 19.

Regarding claim 24, Miyajima discloses in Figs. 14-17 a sealing apparatus for sealing a semiconductor wafer 90 having semiconductor elements on its surface by resin 50, comprising an upper mold 20; and a lower mold 21 having an area where the semiconductor wafer is mounted, the lower mold having an uneven surface in the area,as shown in Figs. 1, 16 and 17; and the upper mold 20 including a cavity 96, 98, 20c on the main surface, and wherein the semiconductor wafer is sandwiched at its periphery by the main surface of the upper mold 20 other than an area where the cavity is formed and the lower mold whereby the resin is not formed on the periphery of the semiconductor wafer.

Regarding claim 25, Miyajima discloses that the cavity is located at a position corresponding to the area, wherein the upper mold further includes a gate, as shown in Fig. 12, connected to the cavity and cull 68 connected to the gate, wherein the gate is located at a position corresponding the periphery of the semiconductor wafer, and where the cavity is formed deeper than the gate.

Regarding claim 26, Miyajima discloses in Fig. 12 that the width of the gate is expanding toward the cavity.

Regarding claims 27 and 28, Miyajima discloses in Figs. 10-15 that the upper mold includes an air vent 96, which is located at a position opposite to the gate, for releasing air in the cavity when the semiconductor wafer is sealed.

Regarding claim 32, Miyajima discloses in Figs. 14-17 a semiconductor device manufacturing mold for sealing a semiconductor wafer 90 having semiconductor elements on its surface by resin 50, comprising an upper mold 20; and a lower mold 21 having an first area where the semiconductor wafer is mounted, the lower mold having an uneven surface, which is formed within a second area, which is in the first area, and wherein the uneven surface is not formed in the periphery of the first area, as shown in Figs. 1, 16 and 17.

With respect to claim 33, how the uneven surface is formed has not been given patentability weight since claimed invention is directed to a device.

Regarding claim 37, Miyajima discloses in Figs. 16 and 17 that the uneven surface is formed by slits 96, 98, 76a, 98a, and 77.

Regarding claim 38, Miyajima discloses in Fig. 16 and 17 that the slits 96 and 76a are formed in parallel to each other.

Regarding claims 39 and 40, Miyajima discloses in Fig. 17 that in the sealing apparatus the area is a first area 21, the slits are formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

Regarding claim 41, Miyajima discloses that the uneven surface is formed by a single spiral slit 98, as shown in Figs. 16 and 17.

Regarding claim 42, Miyajima discloses in Figs. 16 and 17 that the area is a first area, the single spiral slit 98 is formed within a second area, which is in the first area, and the single spiral slit 98 is not extended to the periphery of the first area.

Regarding claim 46, Miyajima discloses in Figs. 14-17 in Figs. 14-17 a sealing apparatus for sealing a semiconductor wafer 90 having semiconductor elements on its surface by resin 50, comprising an upper mold 20; and a lower mold 21 having an area where the semiconductor wafer is mounted, and shock absorbers 78, which are formed under the lower mold 21, buffering stress from the upper mold 20 when the semiconductor wafer is sandwiched by the upper and lower molds, the shock absorbers being disposed symmetrically against the center of the area.

Further with respect to claim 46, Miyajima further teaches the shock absorbers 78 buffering stress to the semiconductor wafer, wherein a part of the shock absorber is exposed in the area.

Regarding claim 48, Miyajima discloses that the shock absorber 78 is formed by a metallic compression spring.

Regarding claims 50, 53, 54, and 94, Miyajima discloses in Figs. 14 and 19, that the shock absorber 78 is a first shock absorber 78,and further comprising a first block 74 having a first recess, the lower mold 21 being contained in the first recess; a second block 76 having a second recess, the first block 74 being contained in the second recess; and second shock absorbers, as shown in Fig. 19 which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

Further with respect to claims 50, and 54, Miyajima further teaches the second shock absorber, which is formed under the second block, buffering stress to the semiconductor wafer.

Regarding claims 52, 56, and 95, Miyajima discloses that the second shock absorbers are formed by a metallic compression spring as shown in Fig. 19.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 4, 5 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyajima.

With respect to claims 4, 5 and 36, Miyamjima teaches the lower mold has an uneven surface or roughness but fails to teach the range for the roughness.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the surface roughness through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyajima in combination with Yamamoto (US pat 6,630,374).

Miyajima discloses in Figs. 14-17 a sealing apparatus for sealing a semiconductor wafer 90 having semiconductor elements on its surface by resin 50, comprising an upper mold 20; and a lower mold 21 having an area where the semiconductor wafer is mounted, the lower mold having an uneven surface in the area, as shown in Figs. 1, 16 and 17; and the upper mold 20 including a cavity 96, 98, 20c on the main surface, and wherein the semiconductor wafer is sandwiched

at its periphery by the main surface of the upper mold 20 other than an area where the cavity is formed and the lower mold whereby the resin is not formed on the periphery of the semiconductor wafer.

Miyajima discloses the claimed invention with the exception of a projection member being formed underneath the center of a back surface the lower mold, which is opposite to the uneven surface, ejection pins formed in the lower mold; the ejection pins pushing the semiconductor wafer up after the semiconductor wafer is sealed by the resin; and the ejection pins disposed symmetrically against the center of the area.

Yamamoto discloses in Figs. IA, 2A, 2C, among others, a sealing apparatus for sealing a semiconductor wafer by resin that comprises an upper mold 1; and a lower mold 2; wherein the structure further comprises a projection member 5 being formed underneath the center of a back surface of the lower mold 2, which is opposite to a top surface where the semiconductor wafer is located; ejection pins 10 formed in the lower mold, the ejector pins pushing the semiconductor wafer up after the semiconductor wafer is sealed by the resin; and the ejection pins being disposed symmetrically against the center of the area, wherein the projection and the ejection pins are taught for the disclosed intended purpose of providing means for effectively applying resin and removing the completed resin sealed semiconductor wafer from the lower mold.

Claims 4, 35, 92, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyajima in combination with Tago (JP 2000-058571).

With respect to claims 4 and 35, Miyajima discloses in Figs. 14-17 a sealing apparatus for sealing a semiconductor wafer 90 having semiconductor elements on its surface by resin 50, comprising an upper mold 20; and a lower mold 21 having an area where the semiconductor wafer is mounted, as shown in Figs. 1, 16 and 17.

Miyamjima teaches the lower mold has an uneven surface or roughness but fails to teach the range for the roughness.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the surface roughness through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Further with respect to claims 4 and 35, Miyamjima appears to fail to teach forming the wafer or substrate directly on the surface of mold or lower mold.

Tago teaches a molding apparatus in which the substrate 57 is mounted directly on a surface of lower mold 60 to prevent reduction in yield. See the English abstract and fig. 1.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Tago into the apparatus of Miyamjima to attain the above benefit.

With respect to claims 92 and 93, how the uneven surface is formed has not been given patentability weight since claimed invention is directed to a device.

Response to Arguments

Applicant's arguments filed 11/28/06 have been fully considered but they are not persuasive. See below.

In repsonse to the applicant's arguments in the paragraph bridging pages 15 and 16 of the response dated 11/28/06, it is submitted that the first area is the entire lower mold 21, the slits 96, 98, 76a, 98a, and 77 form uneven surface within a second area which is located in the first area and the uneven surface is not formed at the periphery or edge of the first area. See figs. 16 and 17.

In repsonse to the applicant's arguments in the paragraphs on page 17 of the response dated 11/28/06, it is submitted that Miyajima teaches a part of each shock absorber 78 is exposed in the area where the semiconductor wafer is to be mounted (see fig. 14, it is the area between 74 and upper part of 78, the area is the portion between the absorber 78 and under the 21 and the exposed area is labeled with a downward arrow). Further, Miyajima further teaches the absorber 78 are disposed symmetrically against the center of the area (vertical in the middle of 74, the area is the portion between the absorber 78).

In repsonse to the applicant's arguments in the paragraphs on page 19 of the response dated 11/28/06, it is submitted that the motivation for incorporating the teaching of Yamamoto is to achieve an effective way to apply and remove completed resin sealed semiconductor wafer from the lower mold.

In repsonse to the applicant's arguments in the paragraphs on page 20 of the response dated 11/28/06, it is submitted that the applicant has the burden of proving criticality of the range of the thickness of the roughness.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP